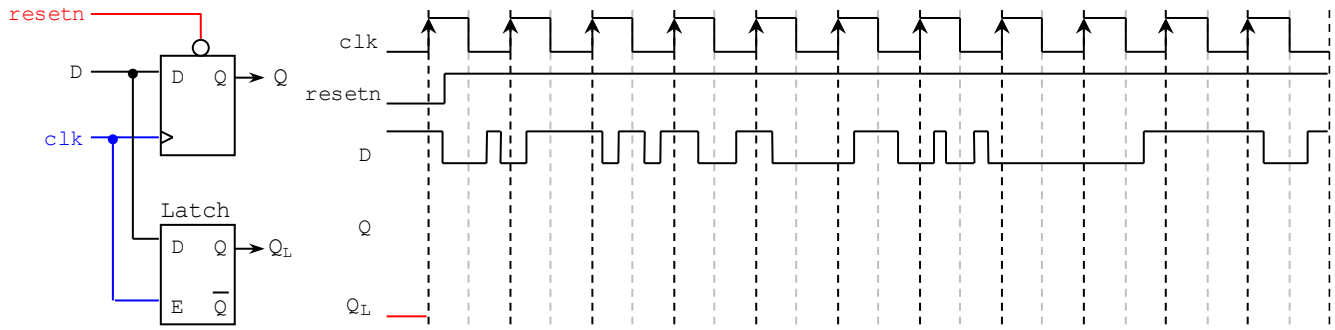
Homework 3

(Due date: November 2nd @ 11:59 pm)

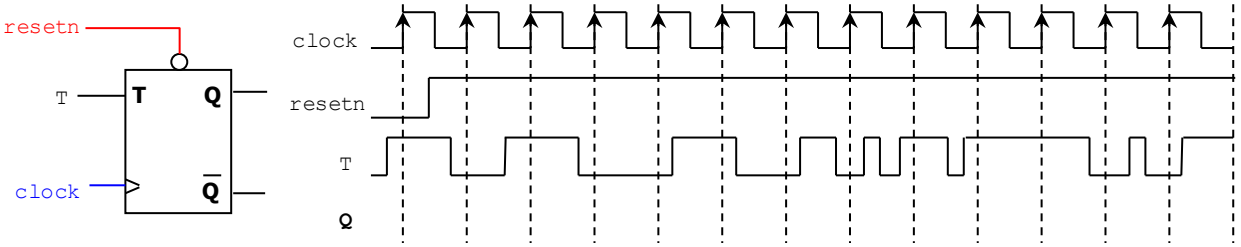
Presentation and clarity are very important! Show your procedure!

Problem 1 (12 pts)

- Complete the timing diagram of the circuit shown below. (7 pts)

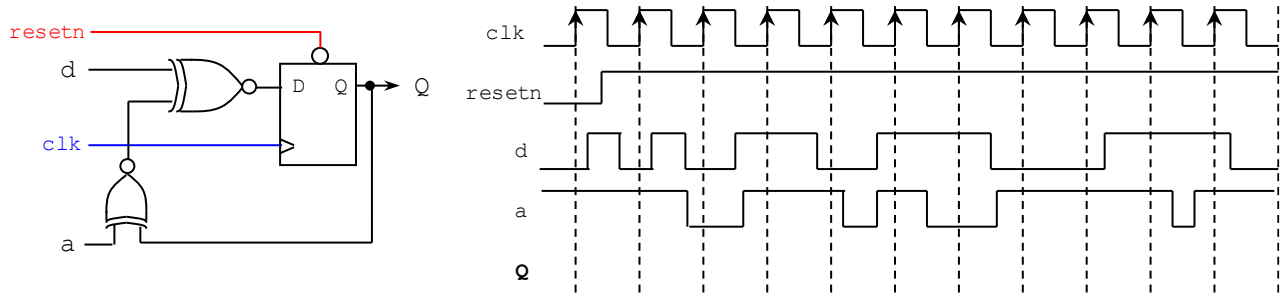


- Complete the timing diagram of the circuit shown below: (5 pts)

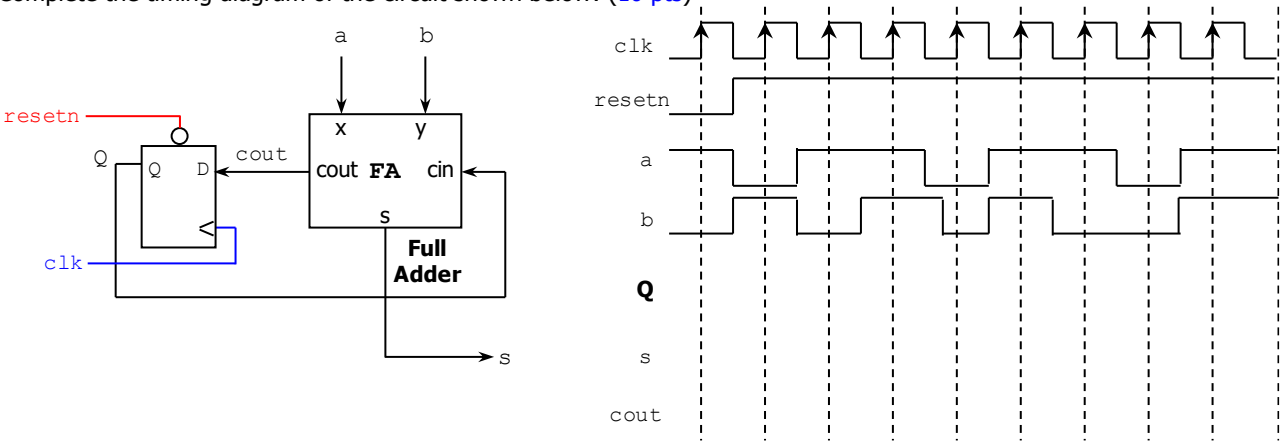


Problem 2 (16 pts)

- Complete the timing diagram of the circuit shown below. Get the excitation equation for Q. (6 pts)



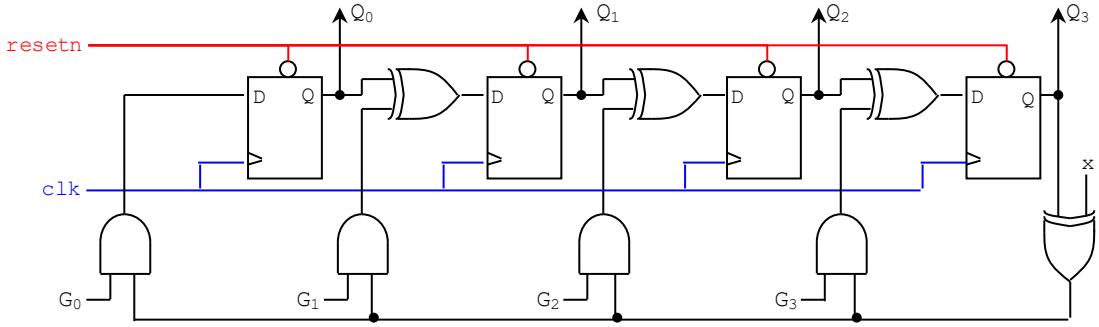
- Complete the timing diagram of the circuit shown below: (10 pts)



PROBLEM 3 (16 PTS)

- With a D flip flop and logic gates, sketch the circuit whose excitation equation is given by:
  - ✓ $Q(t+1) \leftarrow \bar{y}Q(t) + x\overline{Q(t)}$ (4 pts)

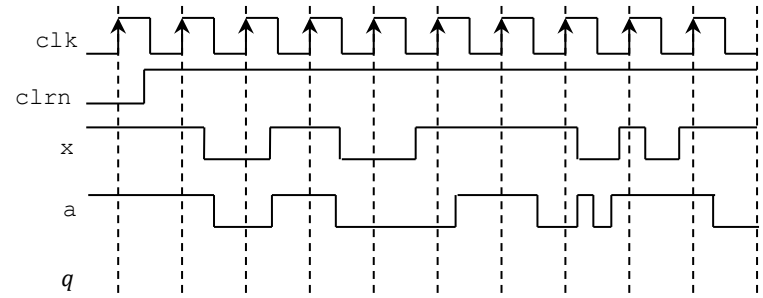
- Given the following circuit, get the excitation equations for each flip flop output $Q = Q_3Q_2Q_1Q_0$ (6 pts)



- Complete the timing diagram of the circuit whose VHDL description is shown below. Also, get the excitation equation for q.

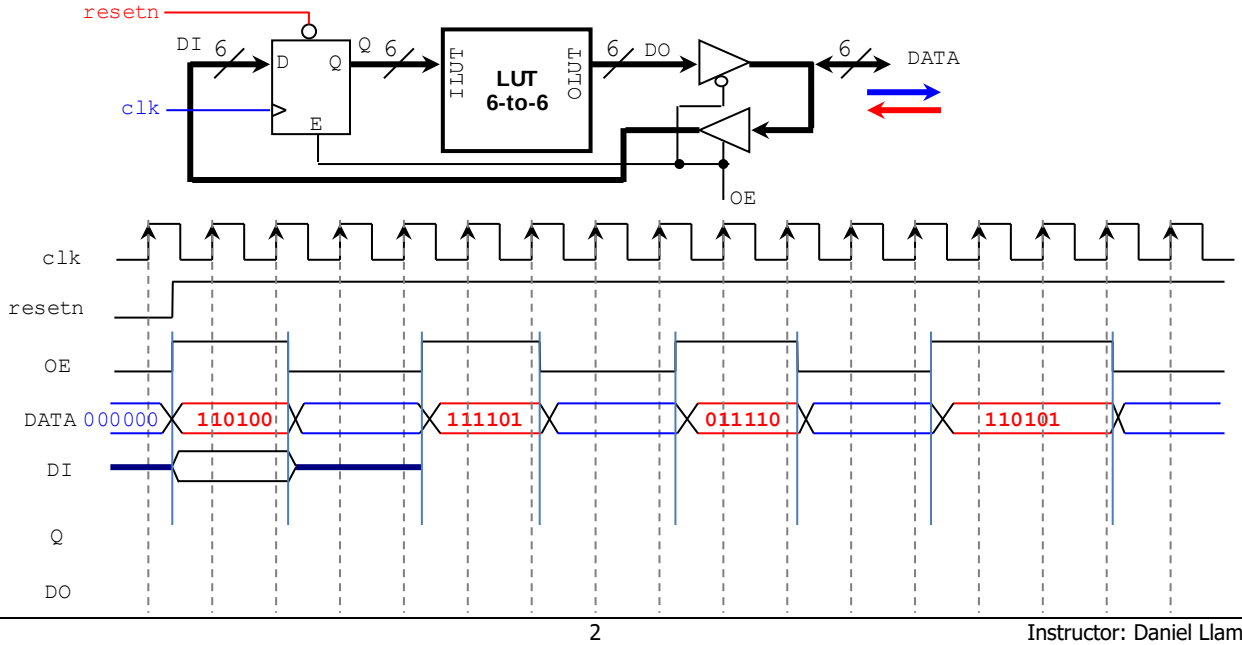
```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port (clrn, clk,x,a: in std_logic;
        q: out std_logic);
end circ;

architecture t of circ is

   signal qt: std_logic;

begin
   process (clrn, clk, x, a)
   begin
     if clrn = '0' then
         qt <= '0';
     elsif (clk'event and clk = '1') then
        if x = '1' then
            qt <= a xnor not(qt);
        end if;
     end if;
   end process;
   q <= qt;
end t;
```

$q(t+1) \leftarrow$



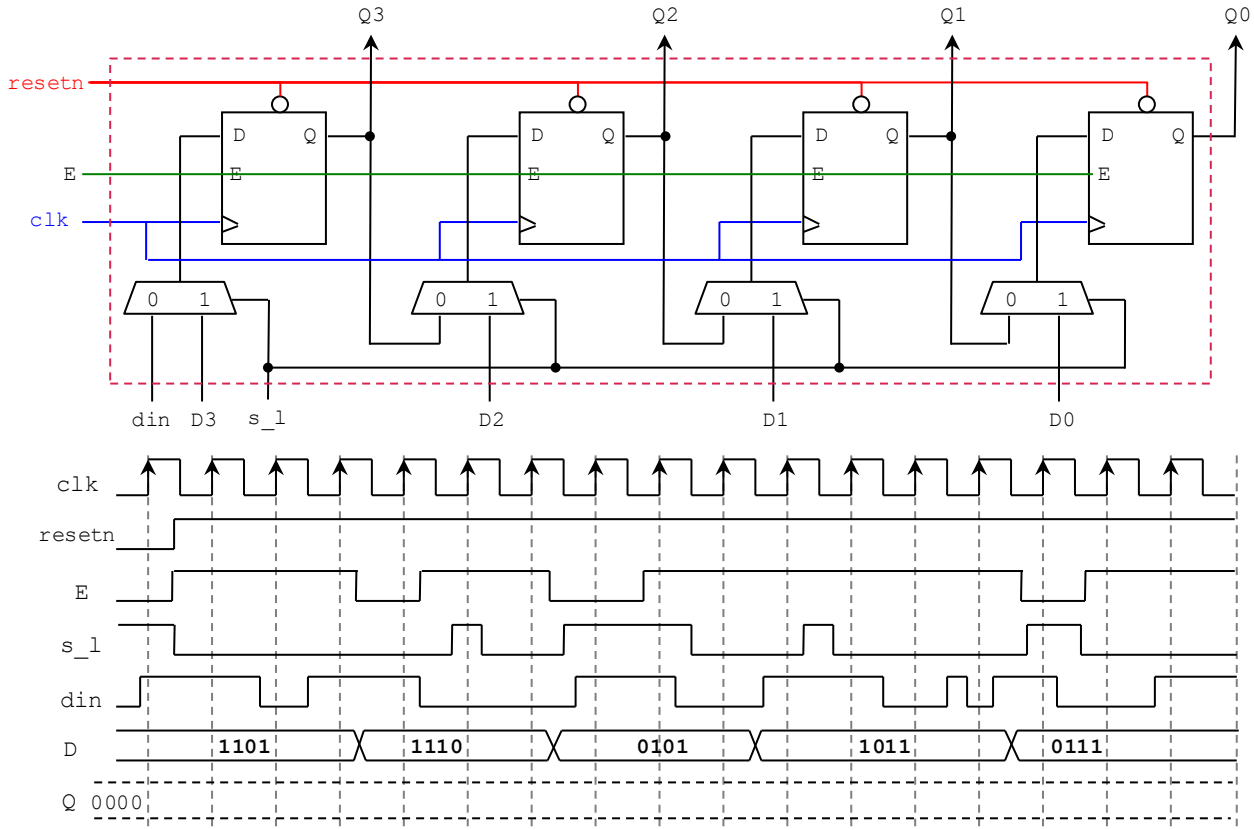
PROBLEM 4 (15 PTS)

- Given the following circuit, complete the timing diagram (signals DO, Q and $DATA$).
  The LUT 6-to-6 implements the following function: $OLUT = \lceil ILUT^{0.85} \rceil$, where $ILUT$ is an unsigned number.
  For example: $ILUT = 35\ (100011_2) \rightarrow OLUT = \lceil 35^{0.85} \rceil = 21\ (010101_2)$



PROBLEM 5 (10 PTS)

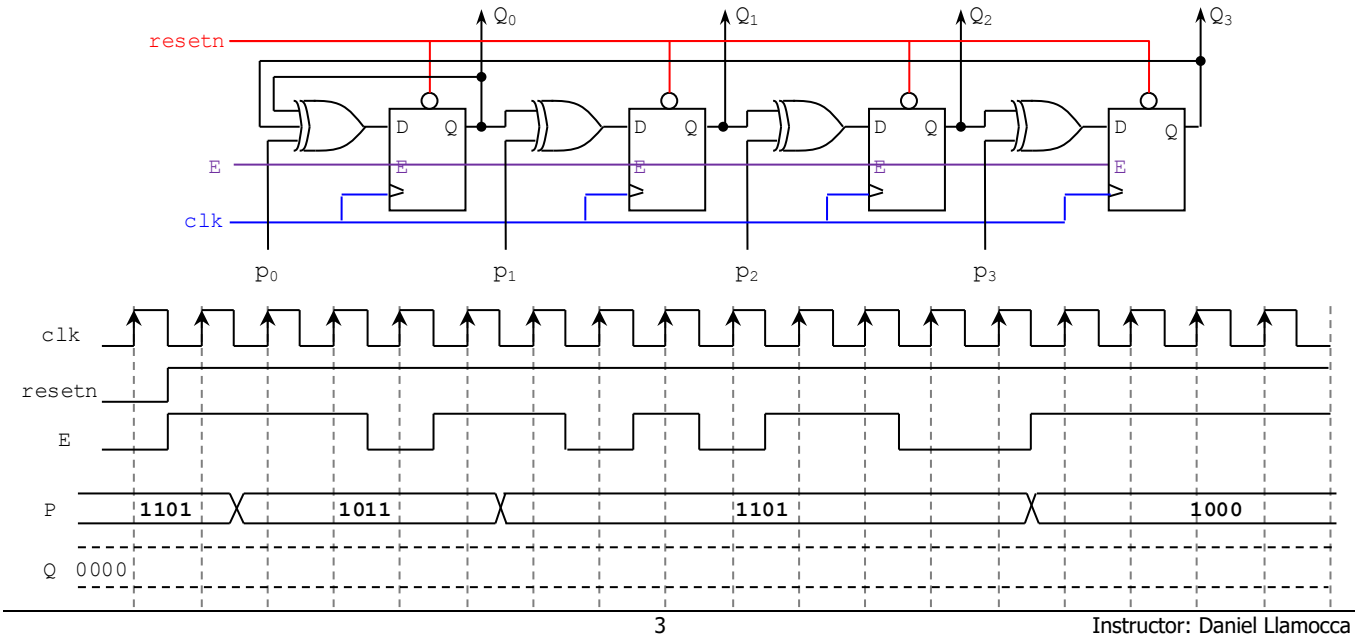
- Complete the timing diagram of the following 4-bit parallel access shift register with enable input.
  When `E=1`: If `s_l=0` (shifting operation). If `s_l=1` (parallel load). Note that $Q = Q_3Q_2Q_1Q_0$. $D = D_3D_2D_1D_0$



PROBLEM 6 (23 PTS)

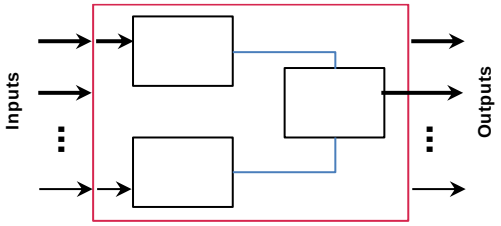
- For the following circuit, we have $Q = Q_3Q_2Q_1Q_0$. $P = P_3P_2P_1P_0$
  - ✓ Write structural VHDL code. Create two files: i) flip flop, ii) top file (where you will interconnect the flip flops and the logic gates). (10 pts)
  - ✓ Write a VHDL testbench according to the timing diagram shown below. Complete the timing diagram by simulating your circuit (Behavioral Simulation). The clock frequency must be 50 MHz with 50% duty cycle. (13 pts)

- Upload (as a .zip file) the following files to Moodle (an assignment will be created):
  - ✓ VHDL code files and testbench.
  - ✓ A screenshot of your simulation showing the results for Q (this is on top of you completing the timing diagram below).



PROBLEM 7 (8 PTS)

- Attach your Project Status Report (no more than 1 page, single-spaced, 2 columns, only one submission per group). This report should contain the initial status of your project. For formatting, use the provided template (`Final Project – Report Template.docx`). The sections included in the template are the ones required in your Final Report. At this stage, you are only required to:
  - ✓ Include a (draft) project description and title.
  - ✓ Include a draft Block Diagram of your hardware architecture.



Block Diagram

- As a guideline, the figure shows a simple Block Diagram. There are input and output signals, as well as internal components along with their interconnection.
  - ✓ At this stage, only a rough draft is required. There is no need to go into details: it is enough to show the tentative top-level components that would constitute your system as well as the tentative inputs and outputs.

- Only student is needed to attach the report (make sure to indicate all the team members).